



RESEARCH DEPARTMENT



REPORT

An experimental helical scan DVTR

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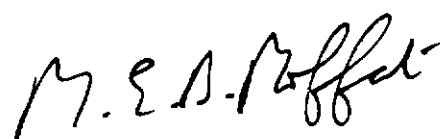
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Summary

This Report describes the design and construction of an experimental DVTR based on a modified helical scan 'C' format machine. The experience gained has enabled the BBC to contribute to discussions to specify an internationally agreed format for digital video recording. The machine has been used within the Department to support research projects.

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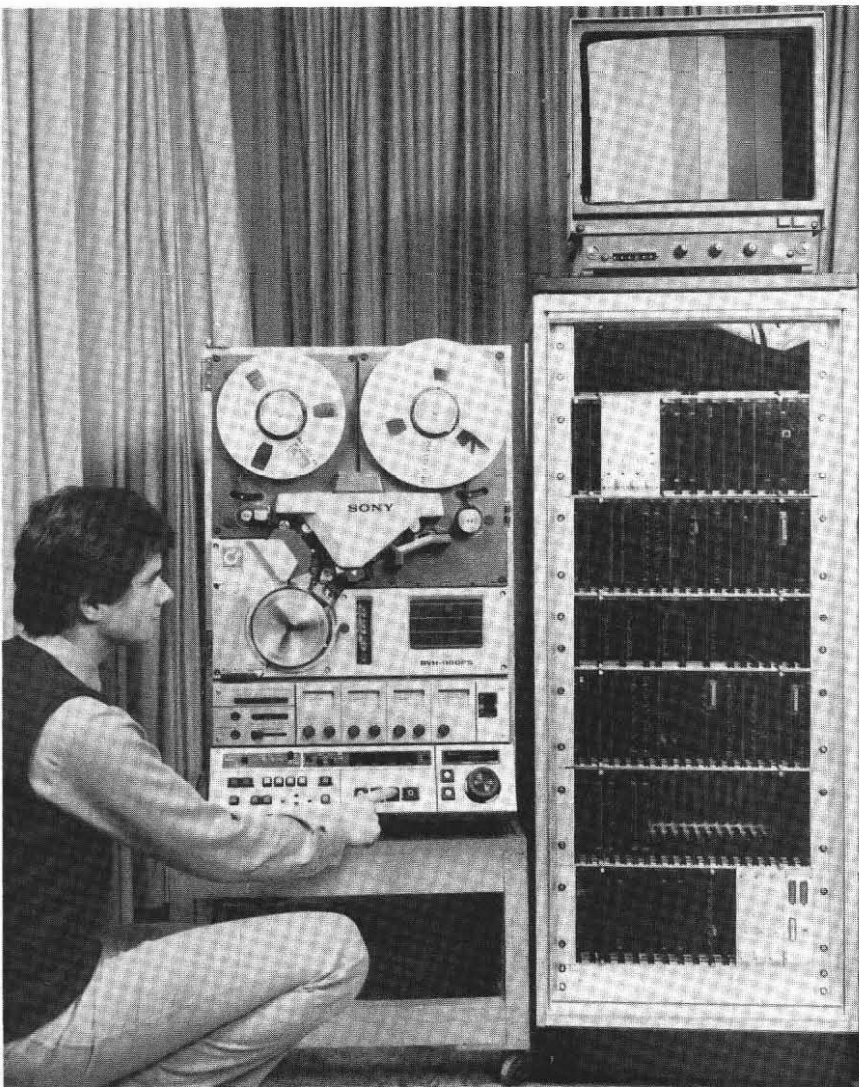


Fig. 1- Overall view of DVTR.

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1. INTRODUCTION

Previous Research Department work on digital video recording has been mainly confined to stationary head machines¹. Whilst acceptable as a research tool, such a machine is not a practical proposition for operational use because expensive multi-track heads are needed, and tape consumption is high because of the high head-to-tape speed.

It is more practical to base a DVTR on helical scan principles. By this means the head-to-tape speed may be increased without a corresponding increase in linear tape speed. Hence higher data rates per head are possible, tracks can be very narrow (leading to high areal packing densities) and tape consumption kept reasonable. Such a machine became available on loan to Research Department from Sony Broadcast, and is used as the basis of an experimental DVTR.

The object of the work described in this Report was to become familiar with the problems of designing and using a helical scan machine for digital video recording so as to be able to contribute to the debate on international standards, and to test relevant ideas. It was not to produce a prototype machine which would be suitable for operational use, nor even to suggest a recording format suitable for such a machine. The major manufacturers of professional video tape recorders have successfully done this, working closely with the European Broadcasting Union (Magnum Group), the SMPTE (DTTR Working Groups) and the CCIR^{2,3,4}. As an additional bonus, the Department should have an experimental machine at its disposal for occasions when it is necessary to record non-PAL signals.

2. DESCRIPTION OF TRANSPORT

The recorder on loan is a modified Sony BVH 1100-PS analogue C-format machine. The head drum is the same size as C-format but the heads have been replaced by one cluster of six digital heads. This was one of a series of experi-

mental head clusters produced to study the performance of multiple heads in helical scan operation. An overall view of the recorder is shown in Fig. 1 and a close-up of the heads in Fig. 2. These lay down six parallel tracks each about 25 microns wide in the space normally occupied by one analogue track. Azimuth recording^{5,6} is employed so no guard band between tracks is needed. About 40 Mbit/s can be recorded on each track, so the total bit rate is 240 Mbit/s. At the time it was not clear how much overhead would be needed for channel coding and error correction. As will be seen, for the implementation described here this bit rate was insufficient to record the whole television picture.

The angle of wrap of the tape round the head drum is about 340° so, as there is only one cluster of heads, a short period of time exists where recording and replay is not possible. This however can largely be absorbed by making the gap (or system drop-out, as it is usually called) coincide with the field blanking of the television signal, and by slightly compressing the data before recording.

The transport is essentially a 'digits in/digits out' device; interconnection with the processing electronics being via balanced ECL lines. A clocking stage has however been added on the input to the transport to improve the accuracy of edge timing. The equalisation, designed and built by Sony, is intended for use with the IBA's 10-8 recording code⁷.

We are using a 20-16 code, devised in Research Department⁸ and which has essentially the same equalisation requirements.

It is only possible to record 7 bits of an 8 bit-per-word coded *Y*, *R-Y*, *B-Y* television signal, sampled at 13.5, 6.75, 6.75 MHz respectively. This is despite all possible economies being made by omitting blanking periods. In addition to this, because of the duration of the system drop-out and the staggering of the heads, only 286 of the active lines can be recorded.

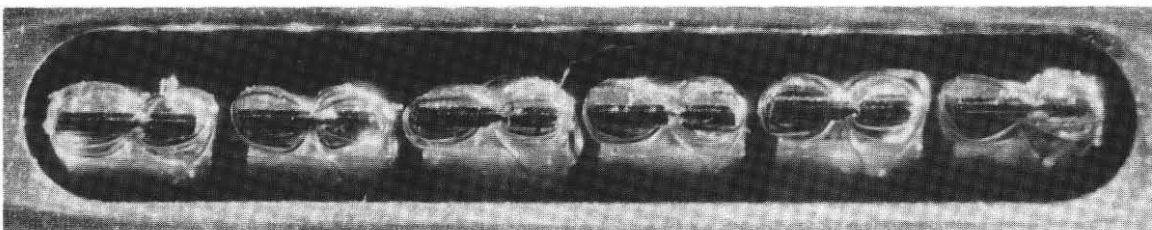


Fig. 2
The cluster
of 6 heads.

3. ANALOGUE *RGB* TO DIGITAL *Y, R-Y, B-Y* CODER

Although the main part of the DVTR is intended to handle digital signals only, it is clearly advantageous to be able to interface with analogue *RGB* signals. Apparatus for encoding analogue *RGB* signals into digital *Y, R-Y, B-Y* form and back again already exists within Research Department. This design, with relatively few modifications, has proved suitable for use with the recorder.

An overall block diagram of the coder is shown in Fig. 3.

Input to the coder is standard 0.7 Vp-p *RGB* signals accompanied by 2Vp-p negative-going synchronising pulses. These *RGB* signals are individually converted to digital form at a sampling rate of 13.5 MHz and with an accuracy of 8 bits per sample. These are then matrixed to give *Y, R-Y* and *B-Y* signals and the *R-Y* and *B-Y* are filtered to reduce the word rate to 6.75 MHz. These coding parameters conform broadly, though not in detail to CCIR Rec. 601⁹. The arithmetic results in 10-bit 2's complement coding which is maintained up to the output of the coder. The *R-Y* and *B-Y* signals are multiplexed together and are converted to offset binary coding. The reason for this is historical, and stems from the use of converted existing equipment.

Fifteen special samples are inserted during line blanking of the *Y* channel. The first of these (coded with all bits set to '0') coincides with the leading edge of analogue line sync. The next ten are encoded to represent the current line number. The remaining four are not used in this application. Coding levels 16 and 240 represent the minimum

and maximum excursions of all signals. In the case of the *Y* signal they represent black and peak white respectively, and for the *R-Y* and *B-Y* signals they are the maximum negative and positive excursions.

4. PROCESSING

Digital signals are input to the recorder as two separate parallel bit streams; a luminance signal, *Y*, and a multiplexed chrominance signal, *R-Y/B-Y*. These channels are maintained independent throughout the record and replay processes, but share the same control data. The signal processing may thus be divided into two nearly identical processing channels; the luminance data being recorded using channels 1, 3 and 5, while the chrominance data is recorded on channels 2, 4 and 6. Each group of tape channels uses heads of like azimuth and therefore suffers little relative timing jitter. Fig. 4 gives a schematic of the various functional blocks found in the luminance signal path.

4.1 Clocking Strategy

The processing for each channel can be further divided into four sections, each under the control of its own set of clock signals; two sections for the record processing and two for the replay. Elastic FIFO (First In First Out) stores are used to buffer the data between the sections. These stores are used to time-base correct the signal on replay and allow for the difference in instantaneous data rates between the real-time video input and output signals and the internal signals associated with recording or replaying the tape. The clock paths are shown schematically in Fig. 4.

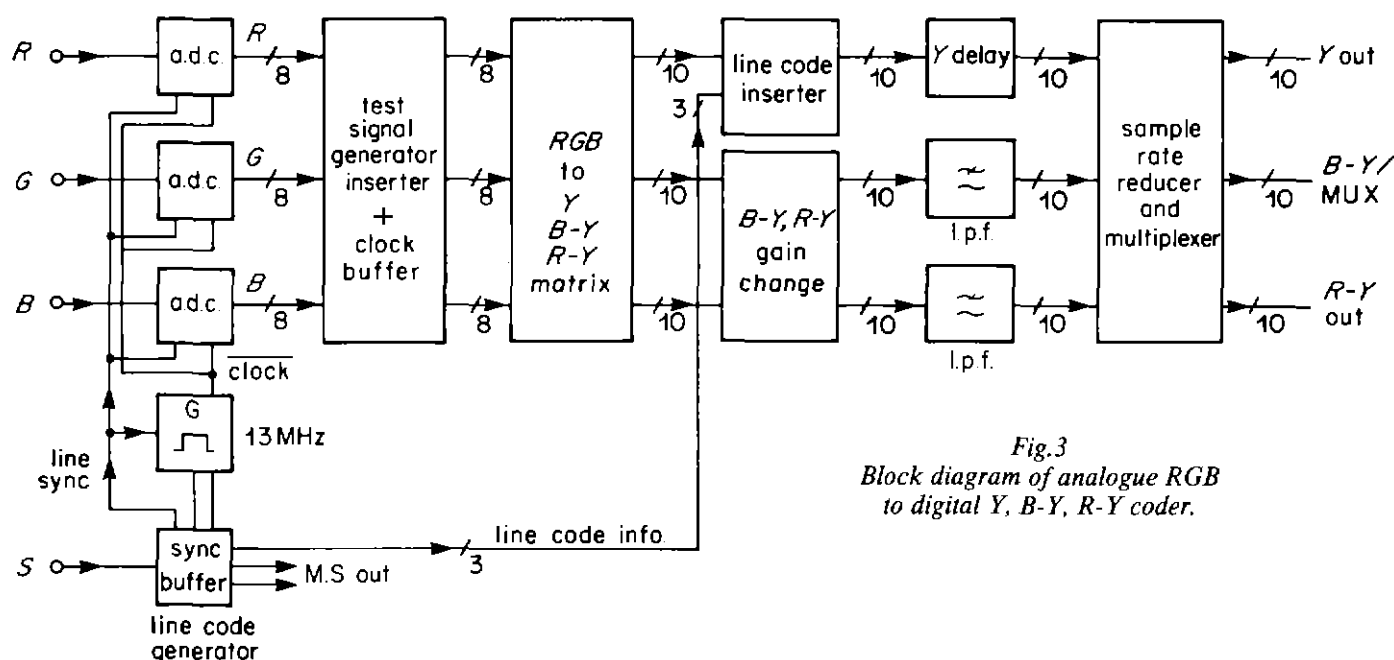


Fig.3
Block diagram of analogue *RGB*
to digital *Y, B-Y, R-Y* coder.

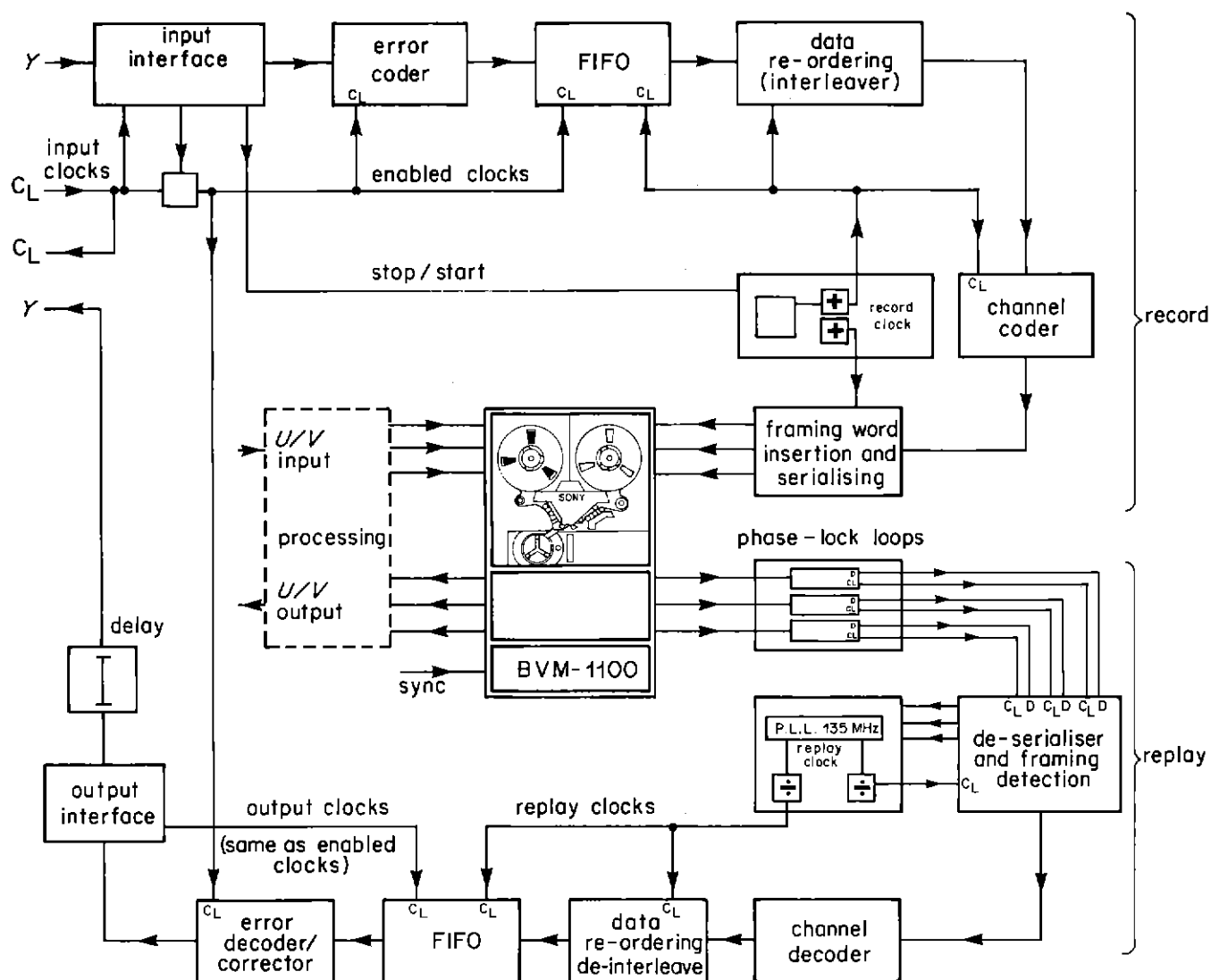


Fig.4 - Block diagram of recorder.

4.2 Signal Processing

The description below applies specifically to the luminance channel but is applicable also to the chrominance channel. The main functions described are shown in Fig. 5.

The input signals are taken to an input interface board which decodes the line numbers included in the luminance signal, to determine the beginning of the active field and the beginning of the active line. These signals control the processing circuits by enabling clocks only while active picture samples are entering the interface.

The 8-bit video bytes are error coded using Wyner Ash error coders which produce one bit of parity overhead per data sample. This parity bit is used to replace the eighth bit (LSB) of the data sample in order to maintain an 8-bit wide processing channel. Hence only 7 bits of the video signal are recorded.

The output from the error coder is then taken to a FIFO store under the control of the clock enabled during active line. The output from the FIFO store is under the control of a separate clock system, derived from the serial clock that records data on tape.

The output data is then interleaved. This function occupies three complex circuit boards for each channel and a common control board. The purpose of interleaving is so that on replay any long bursts of errors caused by tape dropouts are converted into shorter error events which may be successfully corrected by the error decoder. In this case the Wyner Ash code used is capable of correcting one single bit event in every five data words. Thus the interleaver is required to redistribute error events of several thousands of bits such that they only affect one bit per five data words when processed by the error decoder. Complementary processes must clearly be performed on record and replay to ensure the replayed data is

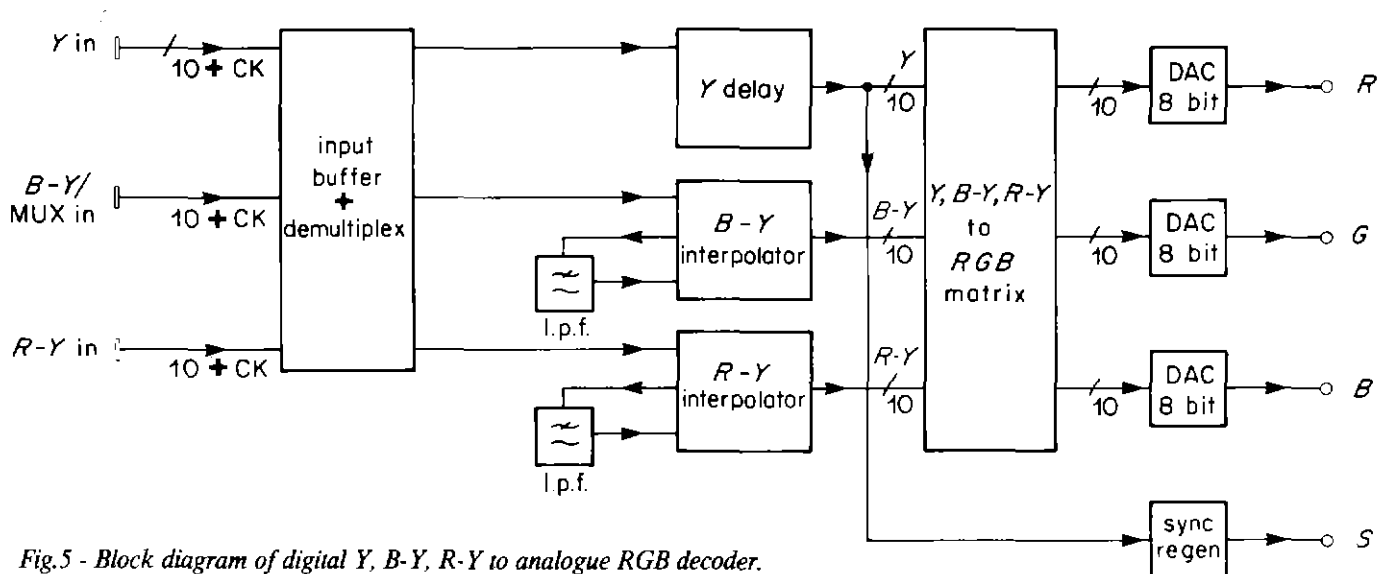


Fig.5 - Block diagram of digital Y, B-Y, R-Y to analogue RGB decoder.

in the correct order for display after the error decoder. In fact the interleaving and de-interleaving processes use similar circuits, and each process is carried out in two stages to minimise the amount of high speed memory needed. The first stage of interleaving distributes individual bits from any one 5-word data block over 256 data words and the second distributes blocks of eight bit-wise-interleaved data words over about 30 television lines.

Within the record channel, the interleaved data is then converted to 16-bit form, by combining pairs of 8-bit words, and is then 20:16 channel coded to produce 20-bit codewords⁸. Framing words are then inserted in the coded data stream. These framing words provide both a reference at the beginning of a line on replay and allow the correct phase of serial-to-parallel conversion to be found. The framing word consists of a bit pattern which can never occur in the serialised coded data stream; making use of an established property of the 20:16 code that these unique framing patterns exist⁸.

The 20-bit words are taken to three serialisers (one for each tape channel). Six channels of serialised data (three for luminance and three for chrominance) are then transmitted to the transport as balanced ECL signals along a 25-way cable. A clock signal is transmitted with the data and used to re-clock the data inside the transport ensuring an accurate and constant mark-to-space ratio for the drive signals to the magnetic heads.

On replay, the six signals from the tape heads are taken first to equalisers and then to slicing circuits to provide balanced ECL signals for transmission to the replay processing. Inside the processing bay each serial signal then passes to a separate phase-locked-loop board. Re-clocked serial signals with their own clock are then taken to two

de-serialising boards; the three signals corresponding to one processing channel being taken to the same board. The correct de-serialising phase is established after checking each bit phase for the bit pattern corresponding to the framing word. The process of serial-to-parallel conversion makes use of a resettable divide by twenty counter, clocked by incoming serial clock. The output from this counter enables the clocking of the serial data from a shift register into a parallel register. For the luminance path, the three parallel signals from the tape channels are combined to form a single twenty-bit wide channel. This then passes to a channel decoder which generates 16-bit data words⁸. These pass to a de-interleaver to put the data in the correct order for error correction and, later, display. The 8-bit video data plus parity bytes are timebase corrected by a FIFO store board. The output from this board is clocked by 'reference' 13.5 MHz clocks, normally derived from those supplied with the input luminance data. This re-timed data is error corrected by the Wyner Ash error decoder.

4.3 Frame Delay

Finally a delay of about half a field is included in the data path and adjusted to time the recorder output correctly relative to station sync, and to permit the reinsertion of station blanking and synchronising pulses.

5. DIGITAL Y, R-Y, B-Y TO ANALOGUE RGB DECODER

A block diagram of the decoder is shown in Fig. 5.

The first task of the decoder is to demultiplex the R-Y and B-Y signals and to convert them to 2's complement coding. This is done using the

sync edge marker in the *Y* channel as a timing reference. The *R-Y* and *B-Y* signals are then interpolated using a filter to increase the word rate to 13.5 MHz, whilst the *Y* signal passes through a compensating delay.

The three signals are next matrixed to *RGB* prior to being converted to analogue form in three identical digital-to-analogue converters. Regeneration of a mixed synchronising waveform is done by reading out the stored parameters of syncs from a ROM, which is addressed by counters. These are locked to the video waveform by detection of the sample with all bits set to '0', corresponding to the leading edge of analogue sync, and by detection of the line numbers. Once the regenerator is locked, it will free run in synchronism with the video signal even if all '0s' and the line numbers are not detected, provided that the clock feed to the unit is not interrupted. The output from the unit is standard 0.7 Vp-p analogue RGB with accompanying synchronising pulses.

6. PERFORMANCE

The performance of the recorder has been rather disappointing. This is for two main reasons. Firstly, the record/replay processing and the head/tape interface in this experimental realisation are only just capable of recording and replaying data at the rates involved, thus demanding that everything be at the peak of its performance for satisfactory operation. Secondly, the tension control, being unchanged from the regular 1" 'C' format VTR, is not really adequate. Bearing in mind that the individual track pitch is 25 microns, that is, less than one eighth of the pitch of the tracks on a PAL 'C' format machine, this is perhaps to be expected. The tension servo cannot be used as no appropriate signal to operate it is recovered when tapes are replayed. As a result, the tape tension varies with time, and tends to be different from one playing of a tape to another. This leads to inaccurate tracking of the heads on the recorded tracks which in turn causes an excessive error rate.

Nevertheless, if the tension is adjusted manually from time to time, using the skew control, the recorder can be used to a limited extent for research purposes.

7. CONCLUSIONS

An experimental digital video tape recorder, based around a modified 'C' format transport, has been described. The machine has been used to support research projects. In the course of constructing the recorder, general digital recording

techniques have been explored and evaluated which have enabled ideas to be contributed to the development of a DVTR format¹⁰.

8. ACKNOWLEDGEMENT

Thanks are due to Sony Broadcast for the loan of the transport complete with heads, and record, replay and equalising circuits. Also for the design of the replay phase-locked-loops, and for their helpful advice during the course of the experiments with the transport.

9. REFERENCES

1. BELLIS, F.A. 1976. An Experimental Digital Television Recorder. BBC Research Department Report No. BBC RD 1976/7.
2. PETERS, J.J. 1985. Journeying Forth with the MAGNUM Group. EBU Technical Review No. 213. Oct. p 223.
3. TODOROVIC, A. 1985. Basis of the EBU Standard on Magnetic Recording of Digital Component Video Signals. EBU Technical Review No. 213 Oct. p 231.
4. ZACCARIAN, P. 1985. Standardisation of the Digital Television Tape Recorder within the Framework of the CCIR. EBU Technical Review No. 213 Oct. p 239.
5. OKAMURA, F. Japanese Patent No. S39-23924
6. KIHARA, N., KHONO, F. and ISIGAKI, Y. 1976. Development of a New System of Cassette Type Consumer VTR. IEEE Trans. on Consumer Electronics. Feb.
7. BALDWIN, J.L.E., BELLIS, R.A. and IVE, J.G.S. UK Patent Application No. G.B. 2001789A.
8. PARKER, M.A. 1985. The 20:16 Block Code for Digital Recording and Transmission Channels. BBC Research Department Report No. BBC RD 1985/1.
9. CCIR Rec. 601. Recommendations and Proposals of the CCIR 1982. XVth. Plenary Assembly, Geneva 1982. Vol. XI - Part 1. Broadcasting Service (Television) pp 271-272.
10. Standard for Recording Digital Television Signals on Magnetic Tape in Cassettes. EBU Document Tech. 3252

